UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,514	02/14/2002	Jeffrey P. Wright	500024.02	3185

7590 01/10/2003

Kimton N Eng
Dorsey & Whitney LLP
1420 Fifth Avenue
Suite 3400
Seattle, WA 98101-4010

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

FN

FN

Office Action Summary	Application No.	Applicant(s)	
	10/055,514	WRIGHT ET AL.	
	Examiner	Art Unit	
	Dennis M. Butler	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. This action is in response to the reissue application filed on February 14, 2002. Claims 1-72 are pending. Claims 53-72 have been added.

2. The original patent, or a statement as to loss or inaccessibility of the original patent, must be received before this reissue application can be allowed. See 37 CFR 1.178.

3. The reissue oath/declaration filed with this application is defective (see 37 CFR 1.175 and MPEP § 1414) because of the following:

A) The declaration fails to contain a statement that **all** errors which are being corrected in the reissue application up to the time of filing of the oath/declaration arose without any deceptive intention on the part of the applicant. See 37 CFR 1.175 and MPEP § 1414. The declaration states that "this error" arose without any deceptive intention.

B) The reference in the declaration to "the enclosed preliminary amendment" is improper because the preliminary amendment was not enclosed with the declaration. The preliminary amendment was received on February 14, 2002 while the declaration was received on June 14, 2002. Applicant is required to make accurate statements in the declaration. Correction is required.

C) Newly added claims 53-72 do not correct the identified error in the declaration. Claims 53-57 appear to be narrower than claim 43 in that they recite the pass gate and that the output node is coupled to ground. Claims 58-72 are directed to entirely different embodiments and do not merely eliminate the pass gate from claim 43 as described in the declaration. In addition, the declaration states that applicant's have the right to claim

that "other means" may be used in the method for generating a pulse. However, applicant's have failed to describe what other means are being used, where there is support in the specifications for using other means and how the new claims correct the error by reciting the other means. Therefore, the declaration does not clearly identify an error that is being corrected by the reissue claims.

4. Claims 1-72 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

5. Claims 11 and 16 are objected to because of the following informalities: the changes made to these claims in the certificate of correction of the parent application must be included in the claims without underlining or bracketing. See MPEP 1411.01. Appropriate correction is required.

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 58 and 61-72 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Elements critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The specification describes the use of a pass gate to perform the steps of transferring and blocking the trigger signal

from an input node to an output node, coupling and decoupling/deactivating the input node to the output node with figure 3, at column 4, lines 25-40 and at column 6, lines 29-39. No other methods of performing the above steps are described in the specification. In addition, applicant has distinguished the invention over the described prior art method by using a pass gate rather than the logic gate in the circuit of figure 1. Applicant describes the advantages of using a pass gate over the prior art circuitry at column 6, lines 29-39. The pass gate is clearly a critical or essential element that is required to perform the above steps as described in connection to figures 1 and 3.

8. Claims 53-72 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant's amendment does not meet 1.173(c) which requires an explanation of the support in the disclosure for new claims. See MPEP 1453. The examiner was not able to find support in the specification for new claims 53-72. Particularly the recitations of the transfer gate and measuring the delay time or time period in claims 64-66 and 68-72. The burden remains on applicant to provide an explanation of support in the disclosure for new claims 53-72.

9. Claims 58-59 and 61-72 are rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Hester Industries, Inc.* v. *Stein,*

Inc., 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement,* 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997); *Ball Corp.* v. *United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. 251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

Claims 58-59 and 61-72 attempt to recapture subject matter that was surrendered in the parent application because applicant did not comment on the examiner's reasons for allowance and have acquiesced to the reasons. See MPEP 1302.14. The above claims do not recite enabling and disabling a pass gate in order to generate the claimed pulse.

10. Claims 58 and 61-72 are rejected under 35 U.S.C. 251 as not being for the same invention as that disclosed as being the invention in the original patent. The specification describes the use of a pass gate to perform the steps of transferring and blocking the trigger signal from an input node to an output node, coupling and decoupling/deactivating the input node to the output node with figure 3, at column 4, lines 25-40 and at column 6, lines 29-39. No other methods of performing the above steps are described in the specification. In addition, applicant has distinguished the

invention over the described prior art method by using a pass gate rather than the logic gate in the circuit of figure 1 because it introduces less delay and therefore is faster than the prior art circuitry. Applicant describes the advantages of using a pass gate over the prior art circuitry at column 6, lines 29-39. Furthermore, applicant has provided no circuit or device for pass gate 120 of the specification. Pass gate 120 appears merely as an oval in figure 3 and the pass gate is defined in terms of the inputs and output. Any device or circuit having the disclosed inputs and output reads on the defined pass gate. Claims 58 and 61-72 are clearly directed to a different invention from the one disclosed in the specification and are not proper reissue claims under 35 U.S.C. 251. See MPEP 1412.01.

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 58 and 63-64 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art.

Per claim 58:

A) The admitted prior art teaches the following claimed items:

1. a trigger signal with clock input signal CLK of figure 1;

2. transferring the trigger signal from an input node (node 20/CLK) to an output node (node 60/IOPU) with figure 2 and at column 1, lines 40-60;

3. propagating the trigger signal through a delay circuit with delay circuit 34 and delayed clock IDCLK of figure 1 and at column 1, lines 43-46;

4. blocking the trigger signal and discharging the output node with figure 2, at column 1, line 58 – column 2, line 6 and at column 2, line 39 – column 3, line 35. Figure 2 shows the output pulse at IOPU. The pulse ends with a low signal. The prior art describes that the low signal is typically 0 volts at column 1, lines 48-49. Therefore, the output node is discharged to 0 volts as shown with IOPU of figure 2.

Per claim 63:

A) The admitted prior art teaches the following claimed items:

1. a trigger signal with clock input signal CLK of figure 1;

2. coupling the input node (node 20/CLK) to an output node (node 60/IOPU) at which the pulse is provided with figure 1 and at column 1, lines 40-60;

3. decoupling the input node from the output node after a period of time with figure 2, at column 1, line 58 – column 2, line 6 and at column 2, line 39 – column 3, line 35;

4. discharging the output node to a first state with the output pulse at IOPU. The pulse ends with a low signal. The prior art describes that the first state is the low state with CLK of figure 2 and at column 2, lines 7-14. The prior art describes that the low signal is typically 0 volts at column 1, lines 48-49. Therefore, the output node is discharged to 0 volts as shown with IOPU of figure 2.

Per claim 64:

The prior art describes a transfer gate with NAND gate 40 of figure 1.

15. Claims 61-62, 67-68 and 71-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art.

Per claims 61 and 67:

The admitted prior art describes the output node is discharged to 0 volts as shown with IOPU of figure 2. In addition, the prior art describes that low logic level signals are typically 0 volts at column 1, lines 48-49. It is well known in the data processing art that 0 volts normally correspond to the ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple

the output node to ground in order to bring the output node to 0 volts for the low logic level signal.

Per claim 62:

Precharging a node to a desired voltage is well known in the data processing art, particularly in the memory art, and it would have been obvious for one of ordinary skill in the art to precharge the output node to a desired voltage level.

Per claim 68:

A) The admitted prior art teaches the following claimed items:

1. a trigger signal with clock input signal CLK of figure 1;

2. coupling the input node (node 20/CLK) to an output node (node 60/IOPU) at which the pulse is provided through a transfer gate (NAND gate 40) with figure 1 and at column 1, lines 40-60;

3. generating a deactivation signal (IDCLK) by delaying the trigger signal and deactivating the transfer gate with delay circuit 34 and delayed clock IDCLK of figure 1, at column 1, lines 43-46, with figure 2, at column 1, line 58 – column 2, line 6 and at column 2, line 39 – column 3, line 35.

B) The claims seem to differ from the prior art in that the prior art fails to explicitly teach coupling the output node to ground to change the voltage level as claimed.

C) However, the prior art describes the output node is discharged to 0 volts as shown with IOPU of figure 2. In addition, the prior art describes that low logic level signals are typically 0 volts at column 1, lines 48-49. It is well known in the data processing art that 0 volts normally correspond to the ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple the output node to ground in order to bring the output node to 0 volts for the low logic level signal.

Per claims 71-72:

The admitted prior art describes the output node is discharged to 0 volts as shown with IOPU of figure 2. In addition, the prior art describes that low logic level signals are typically 0 volts at column 1, lines 48-49. It is well known in the data processing art that 0 volts normally correspond to the ground voltage. Therefore, it would have been obvious for one of ordinary skill in the art to couple the output node to ground in order to bring the output node to 0 volts for the low logic level signal. Precharging a node to a desired voltage is well known in the data processing art, particularly in the memory art, and it would have been obvious for one of ordinary skill in the art to precharge the output node to a desired voltage level.

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler
Primary Examiner
Art Unit 2185